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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,352	12/12/2003	Shunpei Yamazaki	0756-7227	7478

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EXAMINER	
ISAAC, STANETTA D	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 12/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

GA

Office Action Summary	Application No.	Applicant(s)	
	10/733,352	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/24/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the remarks filed on 8/24/05. Currently, claims 1-42 are pending.

Information Disclosure Statement

The information disclosure statement (IDS) was submitted on 8/24/05 was filed after the mailing date of the Office Action on 5/20/05. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-12, 14, 16-31, 33, 35-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al., US Patent 5,789,284 in view of Henley et al., US Patent 6,083,324.

Yamazaki discloses the semiconductor method substantially as claimed. See figures 1A-9C, and corresponding text, where Yamazaki shows, pertaining to claims 1, 10, 22, 30, and 41, a process for producing a semiconductor device, comprising: forming a first semiconductor film **105** having an amorphous structure (figure 1A; col. 6, lines 9-23); adding an element **104** for

promoting crystallization to the first semiconductor film having the amorphous structure (figure 1A; col. 2, lines 50-55; col. 6, lines 1-8, 20-23); conducting a first heat treatment to form a first semiconductor film having a crystal structure (figure 1B; col. 6, lines 24-34); forming a barrier layer **106** over the surface of the first semiconductor film having a crystal structure (for claims 10, 30 and 42, figure 1C; col. 6, lines 43-57); forming a second semiconductor film **107** over the first semiconductor film (over the barrier layer, for claims 10 and 30) having the crystal structure (figure 1C; col. 8, lines 27-35); conducting a second heat treatment to segregate the element for promoting crystallization into the second semiconductor film (figure 1C; col. 8, lines 29-55); and removing the second semiconductor film (figure 1D; col. 8, lines 56-67). In addition, Yamazaki shows, pertaining to claims 2 and 11, wherein the second semiconductor film is formed by sputtering (col. 3, lines 38-43; col. 12, lines 56-63). Also, Yamazaki shows, pertaining to claims 3 and 12, wherein the second semiconductor film is formed by plasma CVD (col. 6, lines 65-67). Yamazaki shows, pertaining to claims 4, 16, 24 and 35, wherein the first heat treatment is conducted by radiation from one or more selected from a halogen lamp, a metal halide, lamp, a xenon arc lamp, a carbon arc lamp, a high-pressure sodium lamp, or a high pressure mercury lamp (col. 6, lines 15-18, ***Note***: the Examiner takes the position that it would be inherent that at least one of the selected lamps would be included, since Yamazaki teaches, that the amorphous silicon films can be formed by plasma CVD, where chambers conventionally include heaters). In addition, Yamazaki shows, pertaining to claims 5, 17, 25 and 36, wherein the first heat treatment is conducted by furnace annealing using an electrical heating furnace (col. 6, lines 25-34; col. 8, lines 31-34, ***Note***: the Examiner takes the position that at least one of the selected heat treatments, since Yamazaki teaches, heating both semiconductor films during a specified amount

of time, where chambers that include furnaces are conventionally used). Also, Yamazaki shows, pertaining to claims 6, 18, 26, 37, wherein the second heat treatment is conducted by radiation from one or more selected from a halogen lamp, a metal halide, lamp, a xenon arc lamp, a carbon arc lamp, a high-pressure sodium lamp, or a high pressure mercury lamp (col. 6, lines 15-18, ***Note***: the Examiner takes the position that it would be inherent that at least one of the selected lamps would be included, since Yamazaki teaches, that the amorphous silicon films can be formed by plasma CVD, where chambers conventionally include heaters). Yamazaki shows, pertaining to claims 7, 19, 27 and 38, wherein the second heat treatment is conducted by furnace annealing using an electrical heating furnace (col. 6, lines 25-34; col. 8, lines 31-34, ***Note***: the Examiner takes the position that at least one of the selected heat treatments, since Yamazaki teaches, heating both semiconductor films during a specified amount of time, where chambers that include furnaces are conventionally used). In addition, Yamazaki shows, pertaining to claims 9, 21, 29 and 40, wherein the element for promoting crystallization is one or more selected from, Fe, Ni, Co, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au (col. 2, lines 51-55). Also, Yamazaki shows, pertaining to claims 14 and 33, wherein the barrier layer is formed by oxidizing the surface of the first semiconductor film having the crystal structure by plasma treatment (col. 6, lines 42-58).

However, Yamazaki fails to show, pertaining to claims 1, 10, 22, 30, and 41, forming a second semiconductor film containing a rare gas element or, adding a rare gas element to the second semiconductor film (for claims 22 and 30). In addition, Yamazaki fails to show, pertaining to claims 23 and 31, wherein the rare gas element is added by any one of ion

implantation and ion doping. Also, Yamazaki fails to show, pertaining to claims 8, 20, 28 and 39,wherein the rare gas element is one or more selected from He, Ne, Ar, Kr and Xe.

Henley teaches, on figures 1A-9C, with emphasis on figures 6A-7, and corresponding text, a polycrystalline silicon layer or an amorphous silicon layer may be used as a gettering layer were noble gas ions are implanted into the layer, and an annealing method is performed (col. 2, lines 1-4, lines 21-47; col. 3, lines 60-64; col. 4, lines 42-45; col. 7, lines 54-67; col. 8, lines 1-29).

It would have been obvious to one of ordinary skill in the art to incorporate, forming a second semiconductor film containing a rare gas element or, adding a rare gas element to the second semiconductor film; wherein the rare gas element is added by any one of ion implantation and ion doping; wherein the rare gas element is one or more selected from He, Ne, Ar, Kr and Xe, in the method of Yamazaki, pertaining to claims 1, 8, 10, 20, 22, 28, 30, 39 and 40, according to the teachings of Henley, with the motivation of creating gettering sites as taught by Henley, for the purpose of removing the impurities for example, metals, such as copper, nickel, silver, gold, or iron, from the first semiconductor film, thereby dramatically improving the crystallized semiconductor film for an active region within a semiconductor device.

Claims 13, 15, 32 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al., US Patent 5,789,284 in view of Henley et al., US Patent 6,083,324 in further view of Bhat et al, US Patent 6,291,888.

Yamazaki in view of Henley discloses the semiconductor method substantially as claimed. See preceding rejection of claims 1-12, 14, 16-31, 33, 35-42 under 35 U.S.C. 103(a).

However, Yamazaki in view of Henley, fail to show, pertaining to claims 13 and 32, wherein the barrier layer comprises a chemical oxide film formed by using ozone water. In addition, Yamazaki in view of Henley, fails to show, pertaining to claims 15 and 34, wherein the barrier layer is formed by oxidizing the surface of the first semiconductor film having the crystal structure with ozone generated by radiation of ultraviolet rays in an atmosphere containing oxygen.

Bhat teaches, a thermal oxide film that may be formed by conventional techniques (col. 6, lines 12-15).

It would have been obvious to one of ordinary skill in the art to, incorporate, wherein the barrier layer comprises a chemical oxide film formed by using ozone water; wherein the barrier layer is formed by oxidizing the surface of the first semiconductor film having the crystal structure with ozone generated by radiation of ultraviolet rays in an atmosphere containing oxygen, in the method Yamazaki in view of Henley, pertaining to claims 13,15, 32 and 34, according to the teachings Bhat, with the motivation of creating an oxide film, whether the oxide film is formed by ozone or thermal oxidation, etc., would prove to be equivalent since the ultimate result would be to create an oxide film as a barrier layer.

Response to Arguments

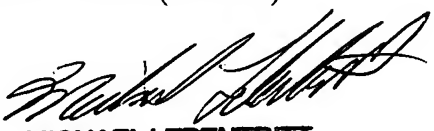
Applicant's arguments, see Response, filed 8/24/05, with respect to the rejection(s) of claim(s) 1-42 under 35 U.S.C.103 (a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Yamazaki et al., US Patent 5,789,284 in view of Henley et al., US

Patent 6,083,324, and Yamazaki et al., US Patent 5,789,284 in view of Henley et al., US Patent 6,083,324 in further view of Bhat et al, US Patent 6,291,888 under 35 U.S.C. 103(a).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER

Stanetta Isaac
Patent Examiner
December 26, 2005